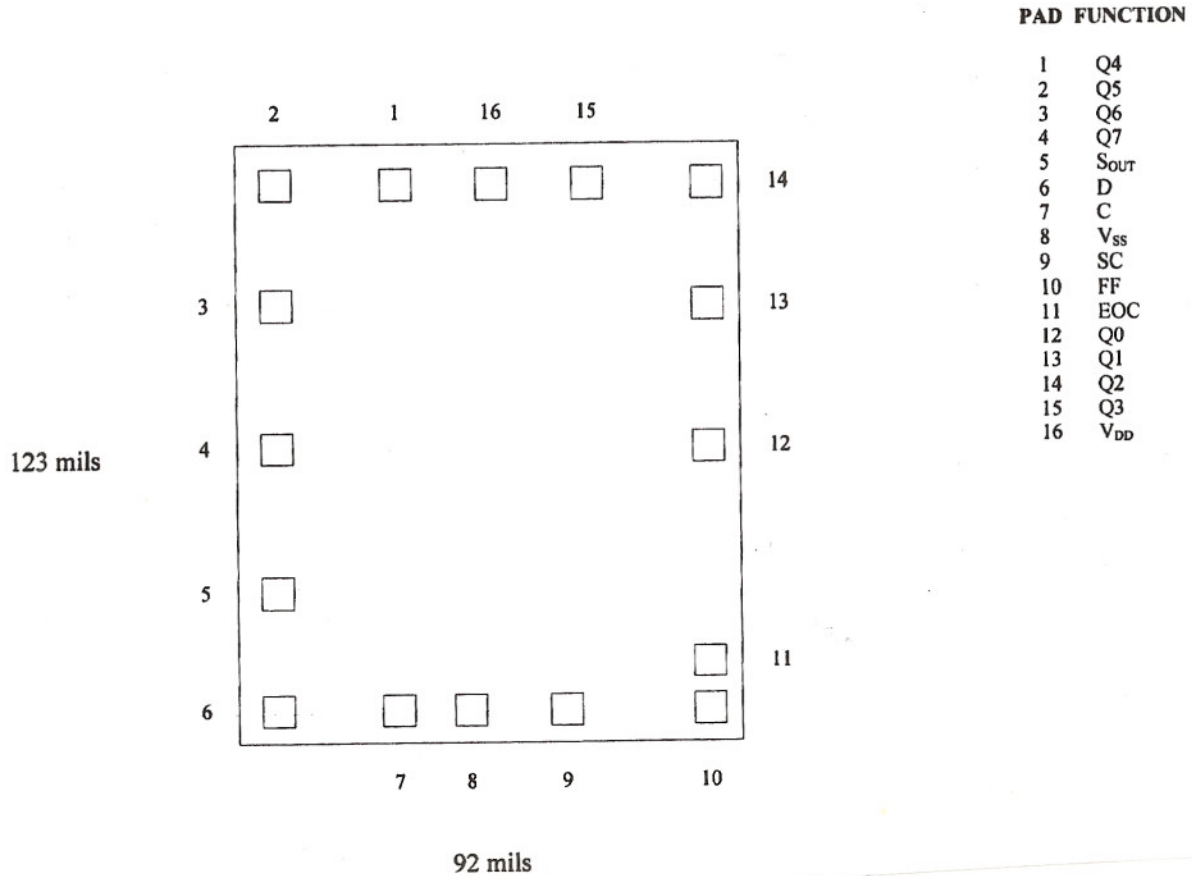




# Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Topside Metal: Al**  
**Backside: Si**  
**Backside Potential: V<sub>DD</sub>**  
**Mask Ref:**  
**Bond Pads (Mils):**

**APPROVED BY:**  
**MFG: Motorola**

**DIE SIZE (Mils): .092"x123"**  
**THICKNESS: .015"**

**DATE: 7/6/04**  
**P/N:CD4559BH**